



Integrated Device Technology, Inc.

# 256KB/ 1MB/ 4MB IDT79R4000 SECONDARY CACHE MODULE BLOCK FAMILY

**PRELIMINARY**  
IDT7MP6074  
IDT7MP6084  
IDT7MP6094

## FEATURES:

- High-speed BiCMOS/CMOS secondary cache module block constructed to support the IDT79R4000 CPU
- Available as a pin compatible family to build 256KB (unified), 1MB (unified) and 4MB (unified or split) secondary caches
- Zero wait-state operation
- Four-word line size
- Operating frequencies to support 50MHz and 75MHz IDT79R4000
- Available as a set of four identical high-density 80-lead (gold-plated fingers) SIMMs (Single In-Line Memory Modules)
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL compatible I/Os
- Single 5V ( $\pm 10\%$ ) power supply

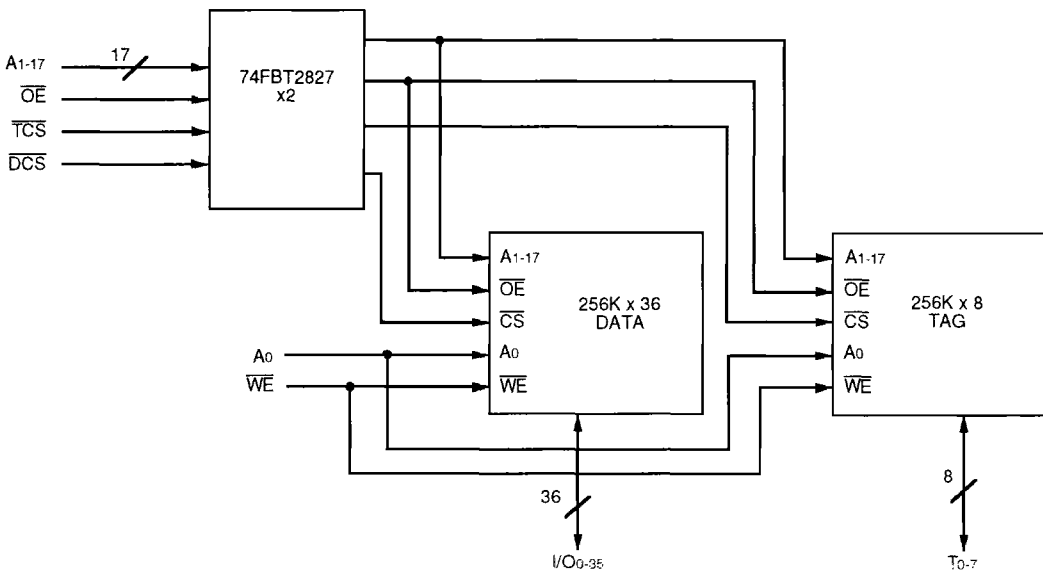
## DESCRIPTION:

The IDT7MP6074 is a 256KB IDT79R4000 secondary cache module block constructed on a multilayer epoxy laminate substrate (FR-4), using eleven 16K x 4 SRAMs and two IDT74FBT2827 drivers. The IDT7MP6084 is a 1MB IDT79R4000 secondary cache module block using eleven 64K x 4 SRAMs, and the IDT7MP6094 is a 4MB IDT79R4000 secondary cache module block using eleven 256K x 4 static RAMs. The IDT74FBT2827 has internal 25W series resistors and BiCMOS I/Os resulting in the fastest propagation times with minimal overshoot and ringing. Four identical cache module blocks comprise a full secondary cache.

The IDT7MP6074/84/94 support use in an IDT79R4000-based system at speeds of 50MHz and 75MHz with zero wait-state operation. These modules support a four word line size. For other line sizes, please consult factory.

All inputs and outputs of the IDT7MP6074/84/94 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation.

## FUNCTIONAL BLOCK DIAGRAM



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**COMMERCIAL TEMPERATURE RANGE**

**AUGUST 1992**

## PIN CONFIGURATION

VCC	2	1	GND
I/O1	4	3	I/O0
I/O3	6	5	I/O2
I/O5	8	7	I/O4
GND	10	9	I/O6
I/O8	12	11	I/O7
I/O10	14	13	I/O9
I/O12	16	15	I/O11
I/O14	18	17	I/O13
I/O15	20	19	GND
I/O17	22	21	I/O16
I/O19	24	23	I/O18
I/O21	26	25	I/O20
GND	28	27	I/O22
I/O23	30	29	VCC
I/O25	32	31	I/O24
I/O27	34	33	I/O26
I/O29	36	35	I/O28
I/O30	38	37	GND
I/O32	40	39	I/O31
I/O34	42	41	I/O33
GND	44	43	I/O35
A0	46	45	WE
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
VCC	54	53	GND
OE	56	55	DCS
A8	58	57	A7
A10	60	59	A9
GND	62	61	A11
A13	64	63	A12
A15	66	65	A14
A17	68	67	A16
T0	70	69	TCS
T1	72	71	GND
T3	74	73	T2
T5	76	75	T4
T7	78	77	T6
GND	80	79	VCC

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SIMM  
TOP VIEW

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

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## PIN NAMES

I/O0-35	Data Inputs/Outputs
T0-7	Tag Inputs/Outputs
A0-17	Address Inputs
DCS	Data Chip Select
TCS	Tag Chip Select
WE	Write Enable
OE	Output Enable
Vcc	Power Supply
GND	Ground

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## CAPACITANCE

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN(D)</sub>	Input Capacitance (Data)	V <sub>IN</sub> = 0V	10	pF
C <sub>IN(A)</sub>	Input Capacitance (A1-15, OE, TCS, DCS)	V <sub>IN</sub> = 0V	10	pF
C <sub>IN(B)</sub>	Input Capacitance (A0, WE)	V <sub>IN</sub> = 0V	100	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

### NOTE:

- This parameter is guaranteed by design, but not tested.

2833 tbl 03

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

### NOTE:

- V<sub>IL</sub> = -1.5V for pulse width less than 10ns.

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## ABSOLUTE MAXIMUM RATINGS

Symbol	Rating <sup>(1)</sup>	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-10 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
I <sub>OUT</sub>	DC Output Current	50	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ )

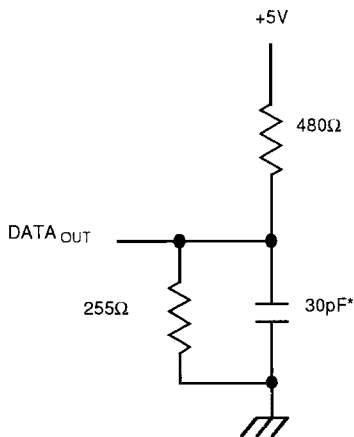
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$ I_{L1} $	Input Leakage (except $A_0, \overline{WE}$ )	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	10	$\mu A$
$ I_{L2} $	Input Leakage ( $A_0, \overline{WE}$ )	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	110	$\mu A$
$ I_{LO} $	Output Leakage	$V_{CC} = \text{Max.}, \overline{CS} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	—	10	$\mu A$
$I_{CC}$	Operating Current	$\overline{CS} = V_{IL}; V_{CC} = \text{Max.}, \text{Outputs Open}$	—	2200	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	2.4	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8\text{mA}$	—	0.4	V

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## AC TEST CONDITIONS

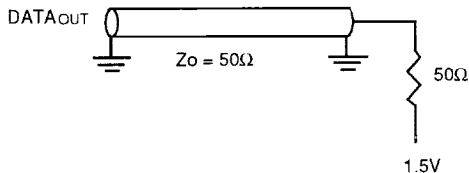
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 - 4

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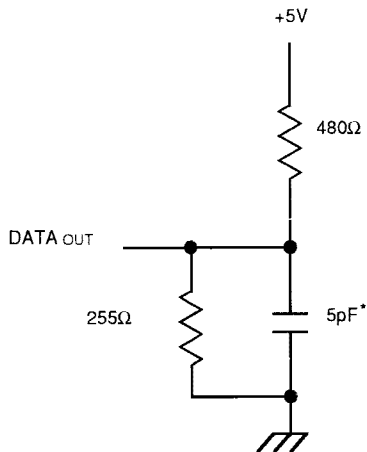
2833 drw 03

Figure 1. Output Load



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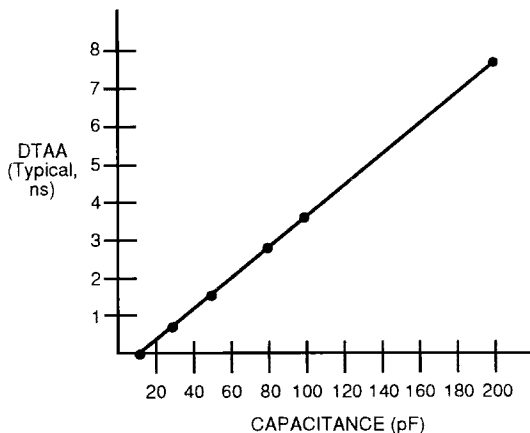
Figure 3. Alternate Output Load



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Figure 2. Output Load  
(for tOLZ and tOHZ)

\* Including scope and jig.



2833 drw 06

Figure 4. Alternate Lumped Capacitive Load,  
Typical Derating

### AC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5V ± 10%, T<sub>A</sub> = 0°C to +70°C)

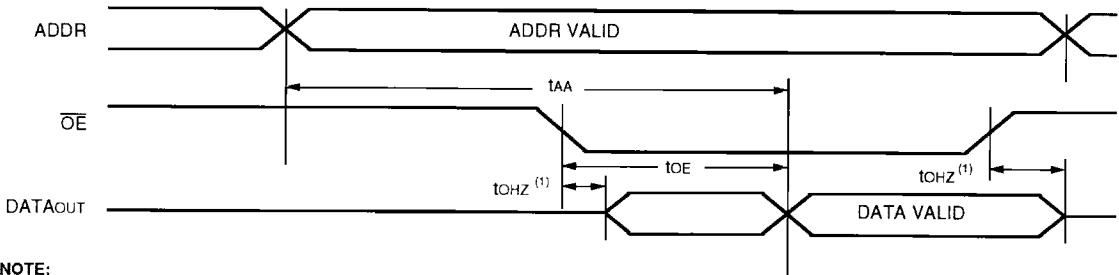
Symbol	Parameter	7MP6074/6084/6094SxxM												Unit
		-12		-15		-17		-20		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>														
tAA	Address Access Time	—	12	—	15	—	17	—	20	—	25	—	30	ns
tA0A	A <sub>0</sub> Access Time	—	10	—	12	—	14	—	16	—	21	—	26	ns
tOE	Output Enable to Output Valid	—	12	—	15	—	17	—	20	—	25	—	30	ns
tOHZ <sup>(1)</sup>	Output Disable to Output in High-Z	—	10	—	12	—	13	—	15	—	17	—	20	ns
tOLZ <sup>(1)</sup>	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
<b>WRITE CYCLE</b>														
tAW	Address Valid to End-of-Write	12	—	15	—	17	—	20	—	25	—	30	—	ns
tA0W	A <sub>0</sub> Valid to End-of-Write	10	—	12	—	14	—	16	—	21	—	26	—	ns
tWP	Write Pulse Width	7	—	10	—	12	—	15	—	20	—	25	—	ns
tDW	Data Valid to End-of-Write	7	—	10	—	12	—	15	—	20	—	25	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns

**NOTE:**

1. This parameter is guaranteed by design but not tested.

2833 tbl 08

### TIMING WAVEFORM OF READ CYCLE<sup>(1)</sup>

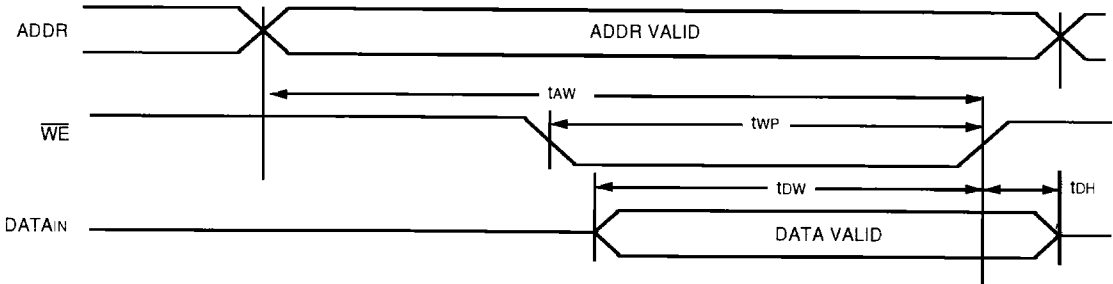


**NOTE:**

1. This parameter is guaranteed by design, but not tested.

2833 drw 07

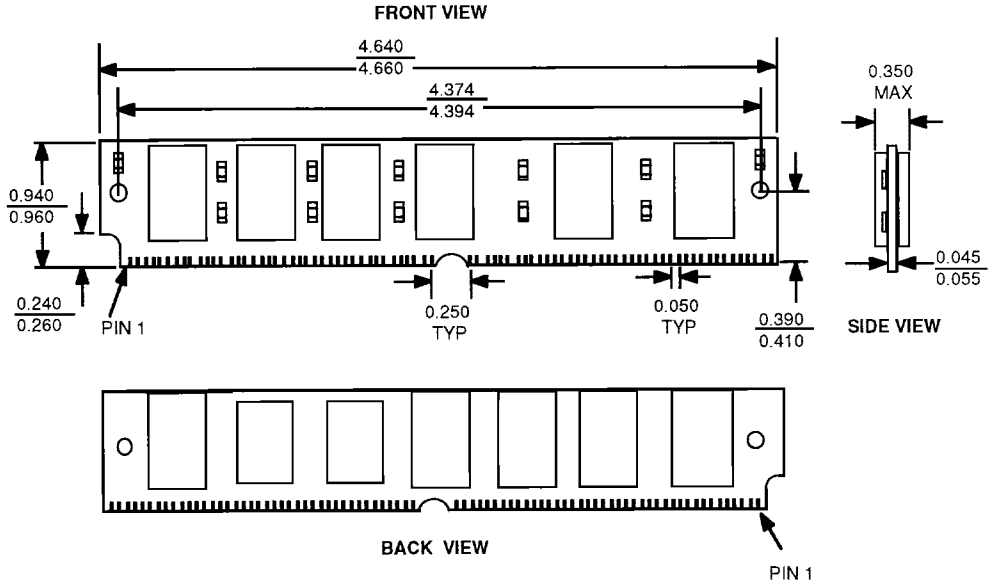
### TIMING WAVEFORM OF WRITE CYCLE



2833 drw 08

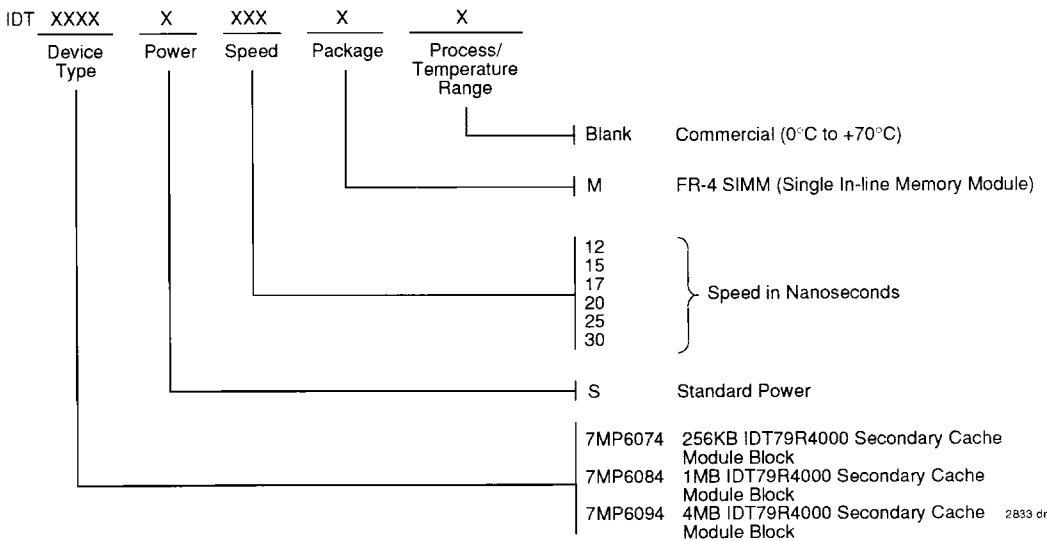
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**PACKAGE DIMENSIONS**



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**ORDERING INFORMATION**



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